REMARKS

The Applicant thanks the Examiner for the careful examination of this application and respectfully requests the entry of the amendments indicated hereinabove. Claims 7-13 are pending and rejected.

Claim 7 positively recites selecting a different gate length for the first gate length using a predetermined design criterion. These advantageously claimed features are not taught or suggested by the patents granted to Ueda et al. and Gardner et al.

Ueda et al. teaches away from the advantageously claimed invention because Ueda et al. teaches that the first gate length is never changed to a different gate length in the location of the first gate (column 10 lines 35-36). Similarly, Ueda et al teaches that the second gate length is never changed to a different gate length within the same location (column 10 lines 43-44). Udea et al. teaches that the transistors of the first basic cell always have a first gate length (column 4 lines 65-67) but never the different gate length of the second basic cell (column 5 lines 1-4 and 20-24). See also column 3 lines 39-45, column 7 lines 14-32, and column 10 lines 34-37 and 40-44.

The Applicant respectfully traverses the statement in the Office Action (page 3) that "Because the source/drain regions are identified the same, it is considered inherent that they posses the same parameters such as doping as well as size." The Applicant submits that Ueda et al. did not intend for common labeling to represent the same size because Ueda et al. specifically states that the gates of figures 1A and 1B – which are labeled with the same numbers – are really different sizes (column 10 lines 35-36, and 43-44).

In addition, the Applicant respectfully traverses the statement in the Office Action (page 3) that "It is considered obvious that Ueda et al. would form the contact to gate centerline spacing substantially the same." The Applicant submits that Ueda et al. teaches that the use of small gate lengths makes the cell smaller and therein increases integration density (column 2 lines 55-57, column 3 lines 6 and 49-51). Ueda et al. specifically teaches that the area used for the first circuit (i.e. size) is less than the area used for the second circuit (column 5 lines 20-22); therefore, by definition, the contact-to-gate centerline spacing is reduced in the cells with the shorter transistor gate length in Ueda et al.

Regarding Claim 9, the Applicant respectfully traverses the statement in the Office Action (page 3) "the first cell and the substitute cell having the same footprint (fig 1(a) and fig 1(b))". The Applicant submits that the cell in figure 1A clearly has a different footprint relative to the cell in figure 1B. Ueda et al. teaches

away from the advantageously claimed limitation because Ueda et al. teaches in FIGS. 2-3 and column 11 lines 16-21 that the integration density is different depending on which cells are utilized.

Gardner et al. does not teach selecting a different gate length for the first gate length as advantageously claimed. Rather, Gardner et al. teaches that the first gate length must remain the same throughout the integrated circuit (column 12 lines 4-10, 36-38, and 40-44, column 5 lines 19-23 and 65-67, column 8 lines 43-46 and 53-54, column 11 lines 8-12 and 17-22). Similarly, when a second gate length is required for a new foundry, only that second gate length is used throughout the integrated circuit (column 3 lines 19-24, column 10 lines 8-10, column 13 lines 53-60). As a result, Gardner does not teach the design of an integrated circuit having both a first transistor having a first gate length and a second transistor having a second gate length, as advantageously claimed.

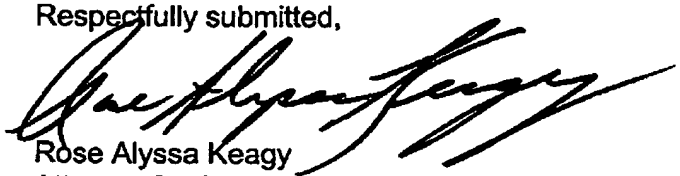
The Applicant respectfully traverses the statement in the Office Action (page 4) that "critical or not critical are a relative terms, logic paths in this prior art are considered critical or non-critical accordingly". The Applicant submits that when all gate lengths are changed by going to a different foundry (such as described in Gardner et al.) there is no consideration of critical versus non-critical.

The Applicant also respectfully traverses the statement in the Office Action (page 4) that "modeling a change of the gate length comprises changing the gate length by a length increment, the length increment less than the length of one grid of a design rule for the IC" is discussed in column 7 of Gardner et al. The Applicant submits that in column 7 Gardner et al. discusses having a cell on the grid of a CAD display; however, there is no teaching regarding the making of a change of less than a grid unit.

Due to the foregoing reasons, the Applicant respectfully traverses the Examiner's rejection of Claim 7 and respectfully asserts that Claim 7 is patentable over Ueda et al. and Gardner et al. Furthermore, Claims 8-13 are allowable for depending on allowable independent Claim 7 and, in combination, including limitations not taught or described in the reference of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



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